Republic of the Philippines
Polytechnic University of the Philippines
COLLEGE OF ENGINEERING
Sta. Mesa, Manila
Tel. No. 716-78-32 to 45

CE VISION

The College of Engineering envisions itself to be a center of excellence in engineering ation.

CE MISSION

The College of Engineering is committed to produce competitive engineers who will serve as catalyst for sustainable growth and development in national and international levels.

CE GOALS

1. Provide Quality education through instruction, advance research and extension services:
2. Produce worldclass professionals as potential industry leaders and job providers
3. Develop and improve facilities through the use of adapted technology and indigenous materials and:
4. Maintain, upgrade and improve facilities through the adaptation of engineering techniques.

OBJECTIVES

1. Strengthen the CE program consistent with global trends;
2. Develop faculty as competent mentors and quality researchers, through advanced studies and other facets of continuing Professional education;
3. Develop the critical thinking and Communication skills of students, giving emphasis to research and extension services;
4. Equip graduates with appropriate knowledge and technical skills imbued with desirable work attitudes and moral values, through enhanced teaching/learning process by using multimedia facilities on top of traditional methods;
5. Create a conducive teaching and learning atmosphere with emphasis to faculty and students' growth and academic freedom;
6. Establish network with educational institutions, Industries, GO's and NGO's, local and international, which could serve as:
   a. Funding sources and/or partners of researches,
   b. Sources of new technology,
   c. Centers for faculty and students' exchange programs and onthe-job trainings, and
   d. Grantees of scholarships/ additional facilities and;
7. Continuously conduct action researches on the Needs of laboratory and other facilities that could Be locally produced or innovated using local Materials and adapted technology

Engr. Engr. Noli Sibayan
CE Chair
Engr. Pedrito Tenerife Jr.
COE Chair
Engr. Ana Liza Publico
ECE Chair
Engr. Faustino Rural
EE Chair
Prof. Joselinda Golpeo
IE Chair
Engr. Jesus Callanta
ME Chair
Engr. Marianito Gallego Jr.
RnD Coordinator
Engr. Carmelita Durias
ES Chair
Engr. Guillermo Bernabe
College Dean

COURSE SYLLABUS
LOGIC CIRCUITS AND SWITCHING THEORY
Revised AY 2011-2012
1st Semester, AY 2012-2013

I. COURSE CODE: COEN 3134

II. COURSE TITLE: Logic Circuits and Switching Theory

III. PRE-REQUISITE: Electronics Devices and Circuits

IV. CREDIT UNITS: 4

V. COURSE DESCRIPTION:

The course includes design and analysis or digital circuits. This course covers both combinational (synchronous and asynchronous) logic circuits with emphasis on solving digital problems using hardwired structures of the complexity of medium and large-scale integration.

VI. OBJECTIVES: At the end of the course the students are expected to:

1.) define the operation of the basic combinational circuits including decoders, encoders, multiplexers, demultiplexers, ALUs, and memory circuits.
2.) study and learn the basic concepts and theories of switching and logic circuits.
3.) develop digital design methodology based on theory, and design realizations, which are straightforward.
4.) acquire skills in the analysis and design of combinational circuits.
5.) understand the work and applications of MSI and LSI devices.

VII. COURSE OUTLINE:

TOPICS	NO. OF HOURS	REFERENCE(S) NO.
I. Classroom Orientation • PUP VMGO • CE VMGO • Classroom Policies	3	1,2,3,4,5
II. Introduction to Digital System • Digital Systems • Analog Systems • Advantages and Disadvantages of Digital Systems • Review of Computer Numbering Systems and Arithmetic Operations	6	
III. Introduction to Digital Circuits • Types of Logic Circuits Combinational Logic Circuits Sequential logic circuits • Building Blocks of Logic Circuits • Logic gates • Constructing Truth table	6	
IV. Boolean Functions and Simplification Process • Boolean function? • Methods of representing Boolean Functions -Logic Diagram -Truth table -Logic Equations -Waveform diagram • Boolean Algebra Laws and Postulates • Boolean Function Simplifications using Boolean Algebra • Canonical Form of Boolean Functions - SOP form (Sum-of-product) - POS form (Product-of-sum) • NAND and NOR Implementation • Boolean Function Simplification using K-mapping approach • Use of Don't Care conditions	10	
V. Analysis of Combinational Logic Circuits • Steps in analysis a combinational logic circuits based on the type of given: - Logic Diagram - Truth Table - Boolean function	3	
VI. Design of Combination Logic Circuits • Steps in designing a combinational logic circuits	3	
MIDTERM EXAMINATION	3	

VII. MSI Devices and Circuits • Adders and Subtractors • Decoders • Encoders • Multiplexers • Demultiplexers • Arithmetic Logic Unit (ALU)	9	1,2,3,4,5
VIII. Introduction to Sequential Logic Circuits	2	
• Types of Sequential Logic Circuits • Clocking and its types • Building blocks of Sequential logic circuits • Latches and Flip-flops • Output wave-forming • Derivation of Excitation table	6	
FINAL EXAMINATION	3	

VIII. ACTIVITIES

- Lecture
- Group Workshops/ Discussions
- Laboratory Experiments
- Seatwork
- Practical Examination
- Written Examinations

IX. REFERENCES

1. Tocci, R. J. (2010). Digital Systems: Principles and Applications (11th Ed.). Prentice Hall
3. Floyd, Thomas (2008). Digital Fundamentals (10th Ed.). Prentice Hall, NJ
4. Mano. M. & Ciletti, M. (2007) Digital Design (4th Ed.). Prentice Hall, NJ
5. Wakerly, J. F. (2005). Digital Design: Principles and Practices (4th Ed.). Prentice Hall.
6. Brown, J. A. & Malvino, A. P. (1992). Digital Computer Electronics (3rd Ed.). McGraw-Hill Companies

X. GRADING SYSTEM

GRADES	PERCENTAGE	/EQUIVALENT
1.0	100-97	Excellent
1.25	96-94	Excellent
1.5	93-91	Very Good
1.75	90-88	Very Good
2.0	87-85	Good
2.25	84-82	Good
2.5	81-79	Satisfactory
2.75	78-76	Satisfactory
3	75	Passing
4.0	74-65	Conditional
5.0		Failure
Inc		Incomplete
W		Withdrawn

Prepared by:

Julius S. Cansino
Course Instructor

Noted by:

Remedios G. Ado
Chairperson

Approved by:

Guillermo O. Bernabe
College Dean

POLYTECHNIC UNIVERSITY OF THE PHILIPPINES

College of Engineering

Computer Engineering Department

Tel No: 713-5968

School Year 2010-2011

COURSE CODE: COEN 3174

COURSE TITLE: Advanced Logic Circuit

COURSE CREDIT: 4 units

PRE-REQUISITE: Logic Circuits Switching Theory

I. COURSE DESCRIPTION:

This course on digital design focuses on different methodologies and styles in hardware modeling with emphasis on the use of hardware description languages (HDLs). It covers very high speed integrated circuit hardware description language (VHDL) fundamental language concepts and elements and the different levels of descriptions such as behavioral and structural.

II. COURSE CONTENT (OUTLINE):

1. Introduction
2. Algorithm State Machines
   - 2.1 ASM Chart
   - 2.2 Control implementation
   - 2.3 Design with Multiplexes
3. Overview of Digital Systems
   - 3.1 Evolution of Digital System Design Methodology
   - 3.2 Different Hardware Description Languages (HDLs)
   - 3.3 History of VHDL
   - 3.4 Advantages and Disadvantages of VHDL
4. VHDL-Related Technologies and Fields
   - 4.1 PLDs
5. Hardware Modeling using VHDL
   - 5.1 Levels of Modeling or Abstraction
   - 5.2 VHDL Model Components or Structural Elements
6. VHDL Language
   - 6.1 Lexical Elements
   - 6.2 Scalar Data Types
   - 6.3 Expressions and Operators
   - 6.4 Control Structures
7. VHDL Language
   - 7.1 Composite Data Types
   - 7.2 Access Types
   - 7.3 File Types
8. Basic Modeling Concepts
9. Subprogram and Packages
10. Algorithmic State Machines
    - 10.1 ASM Charts
    - 10.2 Control Implementation

    Design with Multiplexers

III. STRATEGIES AND METHODS OF TEACHING:

1. Lecture/Discussion
2. Assignment

IV. REQUIREMENTS

- Quizzes
- Examinations
- Class Participations (i.e. Assignment, Seatwork, Recitation, Attendance)

V. REFERENCE:

- Peter Ashenden. The Designer's Guide to VHDL Francisco, CA 2nd edition
- James Armstrong and F. Gail Gray. VHDL Representation and Synthesis. 2nd edition.
- Ulrish Heinkel. The VHDL Reference: A Practical Guide Computer Aided Integrated Circuit Design Includes V AMS
- Douglas Perry. VHDL. 3rd edition.
- IEEE Standard VHDL Language Reference Manual Std 1076-1993-USA
- Ben Cohen. VHDL Coding Styles and Methodologists Ed.
- Zainalabedin Navabi. VHDL: Analysis and Modelling Digital Systems. 2nd edition.
- Kevin Shakill. VHDL for Programmable Logic.

VI. GRADING SYSTEM:

Midterm = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Midterm Exam) 50%
Final = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Final Exam) 50%
General Average = (Midterm) 50% + (Final) 50%

Signed by:

ENGR. REMEDIOS G. ADO
Chairperson, COE Department

DR. MANUEL M. MUHI
Dean, CE

POLYTECHNIC UNIVERSITY OF THE PHILIPPINES

College of Engineering

Computer Engineering Department

Tel No: 713-5968

School Year 2010-2011

COURSE CODE: COEN 3064

COURSE TITLE: Circuits1

COURSE CREDIT: 4 units

PRE-REQUISITE: Physics 2, Integral Calculus

I. COURSE DESCRIPTION:

Fundamental relationships in circuit theory, mesh and node equations; resistive networks, network theorems; solutions of network problems using Laplace transform; transient analysis; methods of circuit analysis.

II. COURSE CONTENT (OUTLINE):

1. Fundamental Relationship in Circuit Theory
2. Resistive Network
3. Mesh and Node Equations
4. Network Theorems
5. Transient Analysis
6. Solution of Network Problems Using Laplace Transform
   Methods of Analysis for Special Circuits

III. STRATEGIES AND METHODS OF TEACHING:

1. Lecture/Discussion
2. Assignment

IV. REQUIREMENTS

- Quizzes
- Examinations
- Class Participations (i.e. Assignment, Seatwork, Recitation, Attendance)

V. GRADING SYSTEM:

Midterm = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Midterm Exam) 50%
Final = [(Q1+Q2+Q3)/3] 30% + CS 20% + (Final Exam) 50%
General Average = (Midterm) 50% + (Final) 50%

Signed by:

ENGR. REMEDIOS G. ADO
Chairperson, CoE Department

DR. MANUEL M. MUHI
Dean, CE

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ANONAS COR. PUREZA STREETS, STA. MESA, MANILA

COPIES OF ALL COURSE SYLLABI

(See Separate Exhibit)

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